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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,358	02/29/2000	Philip A Bourekas	M-7949US	1167

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/515,358	BOUREKAS, PHILIP A	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-8,10-15 and 17-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-8,10-15 and 17-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

AT

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 25th of July 2005 for a request for continued examination (RCE) under 37 CFR 1.114 based on the application No. 09/515358, which the request is acceptable and an RCE has been established. Currently, claims 3-8, 10-15, 17-32 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3-8,10-15 and 17-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al. (US Patent 5,115,506)

As per claim 6, Cohen discloses a processor comprising:

- A set of general purpose registers(fig.1b, 16 ie normal register set); and
- A set of dedicated exception registers(fig.1b, 18 ie alternate register set) that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception registers is substantially dedicated for servicing exception; (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from

18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)

- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.(col.3, lines 8-28), wherein data register D2 as a source of operation(servicing operating system calls) or destination of an operation(servicing interrupts)

As per claim 3, Cohen discloses wherein said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low priority. (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)

As per claim 4, Cohen discloses wherein said processor provides a dedicated vector to said set of exception registers for said exception. (see abstract)

As per claim 5, Cohen discloses wherein there are at least eight exception registers. (col.3, lines 8-28)

As per claim 7, Cohen discloses wherein said processor provides a first dedicated vector to software which uses said portion of said set of exception registers for interrupts and a second dedicated vector to software which uses said another portion of said set of exception registers for servicing operating operating system calls. (col.3, lines 8-28)

As per claim 8, Cohen discloses the processor further comprising a select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register address bit, said select logic

circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers. (col.3, lines 8-40), (col.4, lines 25-45)

As per claim 10, Cohen discloses wherein said at least one set of exception registers is a dedicated set of exception registers. (col.3, lines 29-40), (col.4, lines 8-15)

As per claim 11, Cohen discloses a method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

- swapping a set of general purpose registers for at least one set of exception registers if an exception asserted at said processor is a high priority exception; (col.6, lines 1-11)
- servicing said exception using said at least one set of exception registers if said exception is a high priority exception; (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)
- preserving information from the set of general purpose registers in a memory if said exception is a low priority exception; and (col.2, line 50-col.3, line 7)
- swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception. (col.6, lines 1-11)
- wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of

exception registers without disruption the state of the interrupted task. (col.3 lines 8-28), wherein transparent implies w/o disruption the state)

- wherein during servicing of an exception, a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

As per claim 12, Cohen discloses a method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

- swapping a set of general purpose registers for at least one set of exception registers if an exception asserted at said processor is a high priority exception; (col.6, lines 1-11)
- servicing said exception using said at least one set of exception registers if said exception is a high priority exception; (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)
- preserving information from the set of general purpose registers in a memory if said exception is a low priority exception; and (col.2, line 50-col.3, line 7)
- swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception. (col.6, lines 1-11)

- wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.3, lines 8-28)
- wherein during servicing of an exception a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

As per claim 13, Cohen discloses wherein said first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions. (col.2, line 50-col.3, line 35), (col.4, lines 8-24)

As per claim 14, Cohen discloses a method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

- swapping a set of general purpose registers for at least one set of exception registers if an exception asserted at said processor is a high priority exception; (col.6, lines 1-11)
- servicing said exception using said at least one set of exception registers if said exception is a high priority exception; (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)
- preserving information from the set of general purpose registers in a memory if said exception is a low priority exception; and (col.2, line 50-col.3, line 7)

- swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception. (col.6, lines 1-11)
- wherein said exception is a high priority exception and is either an interrupt or an operating system call, said method further comprising (col.3, lines 8-28)
- providing a first vector and activating at least a portion of said exception registers for said high priority exception when said exception is an interrupts; (col.2, line 50-col.3, line 28), (col.4, lines 8-48)
- providing a second vector and activating at least another portion of said exception registers for said high priority exception when said exception is an operating system calls; and (col.2, line 50-col.3, line 28), (col.4, lines 8-48)
- providing a third vector and not activating said set of exception registers for lower priority exceptions. (col.2, line 50-col.3, line 28), (col.4, lines 8-48)
- wherein during servicing of an exception a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

As per claim 15, Cohen discloses wherein said first vector and said second vector are dedicated vectors and said providing said first vector and providing

said second vector automatically separates said high priority exception from said lower priority exceptions. (col.2, line 50-col.3, line 28), (col.4, lines 8-48)

As per claim 17, Cohen discloses an apparatus for executing tasks and servicing exceptions, said apparatus comprising:

- Means for interrupting a task when an exception is asserted; (col.6, lines 1-11)
- Means for servicing said exception without disrupting the state of the interrupted task, including means for activating at least one set of dedicated exception registers; and (col.4, lines 8-24)
- Means for resuming execution of said interrupted task, including means for deactivating said dedicated exception registers and activating general purpose registers and activating general purpose registers to resume execution of said task. (col.4, line 8-col.6, line 27)
- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.3, lines 8-28)
- wherein during servicing of an exception a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

As per claim 18, Cohen discloses wherein said means for activating comprises a first select logic circuit coupled to said set of general purpose registers and a

second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling said set of general purpose registers. (col.4, line 8-col.6, line 27)

As per claim 19, Cohen discloses wherein said servicing comprises providing a first vector and activating said at least one set of exception registers for said high priority exception, and wherein said providing comprises providing a second vector and not activating said set of exception registers for lower priority exceptions. (col.4, line 8-col.6, line 27)

As per claim 20, Cohen discloses a process comprising:

- A set of general purpose registers; and((col.2, lines 34-37), wherein normal implies general purpose registers)
- A set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when an exception having at least a predetermined priority level is detected by said processor and that are not switched when an exception having a priority less than the predetermined priority level is detected by said processor. (col.6, lines 1-11), (col.4, lines 8-45), (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from 18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)

- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.3, lines 8-28)

As per claim 21, Cohen discloses another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception having at least said predetermined priority level is detected by the processor while said set if dedicated exception registers are switched for at least the subset of said set of general purpose registers. (col.6, lines 1-11), (col.4, lines 8-45)

As per claim 22, Cohen discloses the processor further comprising a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers. (col.3, lines 8-40), (col.4, lines 25-45)

As per claim 23, Cohen discloses a process comprising:

- A set of general purpose registers; and((col.2, lines 34-37), wherein normal implies general purpose registers)
- A set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when an exception having at least a predetermined priority level is detected by said processor and that are not switched when an exception having a priority less than

the predetermined priority level is detected by said processor. (col.6, lines 1-11), (col.4, lines 8-45)

- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls. (col.3, lines 8-28)

As per claim 24, Cohen discloses wherein said set of dedicated exception registers is switched only when an exception, of a first type, having at least a predetermined priority level is detected by said processor and the processor further comprising another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception, of a second type, having at least said predetermined priority level is detected by the processor. (col.6, lines 1-11), (col.4, lines 8-45)

As per claim 25, Cohen discloses wherein servicing said exception using said at least one set of exception registers comprises modifying the values of the registers in said set of exception registers without disrupting the state of the interrupted task. (col.3, lines 8-28)

As per claim 26, Cohen discloses wherein said exception is a high priority exception and is either an interrupt or an operating system call said method further comprising:

- Providing a first vector and activating at least a portion of said exception registers for said high priority exception when said exception is an interrupt; (col.2, line 50-col.3, line 28), (col.4, lines 8-48)

- Providing a second vector and activating at least another portio of said exception registers for said high priority exception when said exception is an operating system call; and (col.2, line 50-col.3, line 28), (col.4, lines 8-48)
- Providing a third vector and not activating said set of exception registers for lower priority exceptions. (col.2, line 50-col.3, line 28), (col.4, lines 8-48)

As per claim 27, Cohen discloses a processor comprising:

- A set of general purpose registers(fig.1b, 16 ie normal register set); and
- A set of dedicated exception registers(fig.1b, 18 ie alternate register set) that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception registers is substantially dedicated for servicing exception at least a subset of rexceptions; (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from 18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)
- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.(col.3, lines 8-28), wherein data register D2 as a source of operation(servicing operating system calls) or destination of an operation(servicing interrupts)

As per claim 28, Cohen discloses a processor comprising:

- A set of general purpose registers(fig.1b, 16 ie normal register set); and
- A set of dedicated exception registers(fig.1b, 18 ie alternate register set) that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception registers is substantially dedicated for servicing exception at least a subset of exceptions; (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from 18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)
- Wherein a portion of said set of exception registers is for servicing interrupts and another portion of said set of exception registers is for servicing operating system calls.(col.3, lines 8-28), wherein data register D2 as a source of operation(servicing operating system calls) or destination of an operation(servicing interrupts)
- wherein during servicing of an exception a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

As per claim 29, Cohen discloses a processor comprising:

- A set of general purpose registers(fig.1b, 16 ie normal register set); and
- A set of dedicated exception registers(fig.1b, 18 ie alternate register set) that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception

registers is substantially dedicated for servicing exception at least a subset of exceptions; (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from 18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)

- Wherein a portion of said set of exception registers is for servicing exceptions and another portion of said set of exception registers is for servicing operating system state and information calls. (col.3, lines 8-28)

As per claim 30, 32, Cohen discloses the portion of said set of exception registers for servicing exceptions is adapted to servicing interrupts. (col.4, lines 8-25)

As per claim 31, Cohen discloses a processor comprising:

- A set of general purpose registers(fig.1b, 16 ie normal register set); and
- A set of dedicated exception registers(fig.1b, 18 ie alternate register set) that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception registers is substantially dedicated for servicing exception at least a subset of exceptions; (col.3, lines 9-28 ie cpu alternating register 16 or 18, either D2 from set 16 or D2 from 18), (col.6, lines 6-11 ie switching from normal to alternate because of first fast interrupt received)
- Wherein a portion of said set of exception registers is for servicing exceptions and another portion of said set of exception registers is for servicing operating system state and information calls. (col.3, lines 8-28)

- wherein during servicing of an exception a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. (col.4, lines 8-55)

Response to Amendment

4. Applicant's amendment filed on 7/25/05 have been fully considered but does not place the application in condition for allowance.

a. In response to applicant's argument that Cohen does not disclose switching for a subset of set of general purpose registers during servicing of an exception. Examiner respectfully disagrees. As Cohen notes at col.3, lines 8-28 and col.4, lines 8-48 discloses cpu alternating the normal register set 16 or the alternate register set 18(fast). There are 7 data registers and 7 address registers from each set. For example D2 register is a subset register of either set. Furthermore, Cohen discloses when a first fast interrupt is received which cause cpu to switch from using the normal register 16 to using the alternate register set 18(col.6, lines 6-11). Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

b. In response to applicant's argument that Cohen does not disclose wherein during servicing of an exception, a subset of registers are not replaced with an alternate set and the registers that are not replaced with an alternate set allow data sharing between exception processing and normal execution. As Cohen notes at col.4, lines 8-

55, discloses the cpu does not return to using the unprimed registers 20 until the first fast interrupt has been completed. And furthermore, Cohen discloses the other registers 24 consist of registers which are not duplicated and can be used by the cpu at any time regardless of whether or not the cpu is carrying out normal operation or interrupt processing. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

September 26, 2005

Khanh Dang
Primary Examiner